

Appl. No.10/565,044; Docket No. US03 0251 US2  
Amdt. dated August 18, 2006  
Response to Office Action dated June 16, 2006

**Amendments to the Claims**

1. (CANCELLED)

2. (CURRENTLY AMENDED) ~~The integrated circuit device of claim 1~~ The integrated circuit device of claim 4, wherein the reference trace is coupled to at least one of the following: a voltage reference, a ground reference.

3. (CURRENTLY AMENDED) ~~The integrated circuit device of claim 1~~ The integrated circuit device of claim 4, wherein, the grounding arch has an area comparable to the area of the integrated circuit device, ~~the semiconductor device die.~~

4. (CURRENTLY AMENDED) An integrated circuit device comprising: a semiconductor device die having a plurality of grounding pads, signal pads, and power pads; and a package for mounting the integrated circuit the semiconductor device die and including a conductive path having at least one reference trace surrounding the integrated circuit the semiconductor device die and having a grounding arch disposed over the semiconductor device die, and ~~The integrated circuit device of claim 1~~ wherein the grounding arch is comprised of metal tape laminated with a dielectric material.

5. (ORIGINAL) The integrated circuit device of claim 4, wherein the grounding arch has a predetermined thickness thereby providing sufficient structure preventing electrical contact between the grounding arch and wire bonds.

6. (CURRENTLY AMENDED) ~~The integrated circuit device of claim 1~~ The integrated circuit device of claim 4, wherein the grounding arch is coupled to at least one grounding location on the integrated circuit device, wherein the grounding location includes, ~~the grounding trace~~ the reference trace and grounding pads on the semiconductor device die.

7. (CURRENTLY AMENDED) The integrated circuit device of claim 6 wherein the grounding location ~~further includes~~ further includes a location about a center region ~~on the integrated circuit device, the semiconductor device die.~~

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8. (ORIGINAL) The integrated circuit device of claim 5 wherein the grounding arch comprises conductors of a highly conductive material selected from: copper, gold, silver, aluminum and an alloys thereof.

9. (ORIGINAL) The integrated circuit device of claim 5 wherein the highly conductive material is in a form including solid tape, mesh, and woven wire bonds.

10. (CURRENTLY AMENDED) ~~The integrated circuit device of claim 1~~ The integrated circuit device of claim 6, wherein the grounding arch is coupled to the grounding location with at least one of the following: conductive glue, solder, eutectic metal bond, a thermo-compression bond.

11. (CURRENTLY AMENDED) ~~The integrated circuit device of claim 3; The integrated circuit device of claim 4~~, wherein the dielectric material is selected from at least one of the following: epoxy, polyimide, polyamide, solder mask, PTFE, and TEFLON™.

12. (CANCELLED)

13. (CURRENTLY AMENDED) A method for controlling impedance of bond wires in packaging a semiconductor device die in a package. the method comprising: defining locations of signal and power/ground pads on the device die; defining grounding trace locations on the package; bonding the signal pads and power/ground pads of the device die; providing a conductive path including a ground arch over the bond wires and grounding trace locations and encapsulating the device die and ground arch, and ~~The method of claim 12 wherein providing a conductive path further includes, rotating the package a pre-determined amount; and providing an additional ground arch.~~

14. (ORIGINAL) The method of claim 13 wherein the pre-determined amount is about 90°.

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15. (ORIGINAL) The method of claim 13, wherein providing an additional ground arch is a function of device design, package size, number of wire bonds, and a desired impedance.

16. (ORIGINAL) The method of claim 15, wherein the desired impedance is function of a ground arch distance from a wire bond.